Regarding the Attorney Docket Number

Applicant has amended the Attorney Docket Number for the present application to be consistent with the undersigned's office practice. Applicant respectfully requests that the PTO records be amended accordingly.

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1-41 stand rejected under 35 U.S.C. §102(e) as being anticipated by Razon. The present invention, as defined by independent claim 1, is directed to a method for selecting components for a matched set. The method includes electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly, simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer, dicing the wafer-interposer assembly into a plurality of chip assemblies, and selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing.

With reference of figure 1 of the application, Applicant describes the wafer-interposer assembly as follows:

> Wafer-interposer assembly 10 allows for the simultaneous testing of groups of chips 24 or all of the chips 24 of wafer 18. Simultaneous testing provides added efficiency to the testing process as numerous aspects of the functionality and performance of chips 24 may be tested. Importantly, this type of simultaneous testing allows for

a determination of which chips 24 match up best with one another. This allows for optimization of the overall performance of specific matched sets as well as the overall performance of all the matched sets made from chips 24. Page 12, line 22 - page 14, line 7.

Applicant continues the description with the following:

After electrical connection to the testing unit 82, wafer-interposer assembly 80 can be used to run the chips on wafer 92 through any number of tests including a complete parametric test, a burn-in or whatever subsets thereof are deemed necessary for that particular chip design. During the course of testing, signals may be sent to individual chips, groups of chips or all of the chips to test each function of the chips which may ideally occur across a range of conditions, so as to simulate real world operation. Testing unit 82 may incorporate a heating and cooling apparatus for testing the chips across a range of temperatures including burn-in testing. Testing unit 82 may also incorporate a device for vibrating or otherwise mechanically stressing the chips.

More specifically, wafer-interposer assemblies 80 of the present invention may be used to select chips from wafer 92 that will be used in a matched set of chips. For example, the testing may include performance tests over a range of temperatures, testing for leakage currents, testing for offset voltages, gain tracking, bandwidth and the like to determine which of the chips from wafer 92 could be included in a matched set with other chips from wafer 92 to achieve optimum performance. Alternatively, the testing may result in giving each of the chips a grade for speed or other performance characteristics such that chips of a particular grade may be matched with other chips of that same grade. Additionally, the testing may result in a non-conformance or mismatch determination wherein certain chips may not be matched with certain other chips. Certain chips may alternatively be designated as incompatible with any other chips. Page 18, line 5 - page 19, line 10.

Applicant's wafer-interposer assembly enables the simultaneous testing of groups of chips to provide an optimization of the overall performance of specific matched sets. Accordingly,

the wafer-interposer assembly of the present invention enables the selection of chips from the wafer that will be used in a matched set of chips based upon the simultaneous testing.

Applicant respectfully submits that the method for selecting components for a matched set as recited in claim 1 is neither disclosed nor suggested by Razon. In particular, Razon neither discloses nor suggests simultaneously testing of at least two integrated circuit chips of a semiconductor wafer that is a part of a wafer-interposer assembly or selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing.

Razon discloses a wafer level packaging technique using a variation of a Tape Automated Bonding (TAB) technique in which the devices are packaged at the wafer level using one interposer sheet per die. As a part of the technique, Razon discloses wafer level testing that occurs prior to the attaching of the interposers. Razon describes his wafer level testing procedures as follows:

> Prior to the integration of the devices 101, each chip on wafer 100 is tested using conventional electrical test equipment, and any defective chips are identified. The tests determine whether each individual chip 100a, 100b etc. on the portion of the semiconductor wafer 100 complies with a predetermined set of acceptance criteria. Preferably, **only those chips which comply with the electrical acceptance criteria are included in the plurality of chips that are processed in the manner shown in FIGS. 2A-2G.** Any chips that are determined to be

> defective may be marked prior to the package fabrication process, and remain unpackaged on the wafer until the completion of the fabrication and cutting steps shown in FIGS. 2A-2G. Following the cutting (dicing) step of FIG. 2F, the defective chips may be discarded. Emphasis added. Column 4, lines 42-55.

Razon states that conventional electrical testing, for example, using a set of probes, is performed prior to the integration of the devices 101 of figures 2A-2G. Razon states that "only those chips which comply with the electrical acceptance criteria are included in the plurality of chips that are processed in the manner shown in FIGS. 2A-2G." Therefore, testing occurs prior to the implementation of the interposers 106 of figure 2B.

Moreover, figure 2B of Razon illustrates a semiconductor wafer 100 containing two chips 100a, 100b, each having an interposer 106a, 106b, respectively. Accordingly, the interposers 106 of Razon are chip level interposers, not wafer level interposers as claimed by Applicant. Furthermore, as chip level interposers do not electrically interconnect the chips, i.e., interposer 106a is only electrical interconnected to chip 100a, an interposer of Razon cannot provide for the simultaneous testing of multiple chips as claimed by Applicant. Therefore, the wafer level testing of Razon can not be equated with Applicant's simultaneous testing of at least two chips on a wafer that is a part of a wafer-interposer assembly and selecting at least two of the chip

assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing as recited in claim 1. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(e) rejection and allowance of claim 1.

Claims 2-17 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2-17 is respectfully requested.

The present invention, as defined by independent claim 18, is directed to a method for assembling a matched set. Similar to claim 1, claim 18 includes limitations directed to providing a semiconductor wafer having a plurality of integrated circuit chips, coupling the wafer to an interposer to form a wafer-interposer assembly and simultaneously testing pairs of the integrated circuit chips of the wafer for inclusion in a matched set based upon the testing. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §102(e) rejection and allowance of claim 18.

Claims 19-34 depend from independent claim 18 and introduce further limitations in combination therewith. Therefore, the allowance of claims 19-34 is respectfully requested.

The present invention, as defined by independent claim 35, is directed to a matched set assembled by the method as recited in claim 18. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §102(e) rejection and allowance of claim 35.

The present invention, as defined by independent claim 36, is directed to a matched set of integrated circuit chips. Similar to claim 1, claim 36 includes limitations directed to simultaneously testing first and second chip assemblies that are a part of a wafer-interposer assembly for inclusion in a matched set based upon the testing. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §102(e) rejection and allowance of claim 36.

Claims 37-41 depend from independent claim 36 and introduce further limitations in combination therewith. Therefore, the allowance of claims 37-41 is respectfully requested.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 1-41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lam in view of Applicant's disclosure on pages 2-4 of the Specification. As previously discussed, Applicant's invention, as defined by independent claim 1, is

directed to a method for selecting components for a matched set. The method includes simultaneously testing at least two of the integrated circuit chips in a wafer-interposer assembly and selecting at least two of the chip assemblies for inclusion in a matched set based on the simultaneous testing of the corresponding two chips.

Applicant respectfully submits that the method for selecting components for a matched set as recited in claim 1 is neither disclosed nor suggested by Lab. Lam discloses a method for packaging a semiconductor die at the wafer level using one interposer sheet for the entire wafer. Lam describes his testing procedures as follows:

> At this point, electrical testing may be conducted on the wafer/interposer assembly 39 since the wafer assembly 39 contains finished dice arranged in a matrix format. This allows for parallel testing which can be conducted at the wafer level and can provide savings in testing time and cost. Then the wafer/interposer assembly 39 is diced, or singulated, such as along line 60, to form individual chip-size BGA packages 70, 72. A common technique for the singulation is to use a wafer saw with diamond or resinoid saw blades. With reference to FIG. 9, the finished BGA package 70 of the present invention has the same footprint as the individual silicon die, as no extra space is needed to accommodate wirebond leads or larger substrate bases. In this way, the integrated circuit package of the present invention provides the advantages of a smaller package size and the convenience of packaging at the wafer level. Column 5, lines 19-37.

Assuming *arguendo* that Lam discloses simultaneous testing of at least two integrated circuit chips of a semiconductor wafer, as stated by the Examiner, Lam does not disclose or

suggest selecting at least two of the chip assemblies for inclusion in a matched set based upon the simultaneous testing.

This deficiency is not cured by the application of Applicant's Background of the Invention. Applicant respectfully submits that the method for selecting components for a matched set as recited in claim 1 is neither disclosed nor suggested by the combination of Lam and Applicant's Background of the Invention. In particular, the step of selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing is not found in the combination.

Applicant traverses the Examiner's characterization of the Background of the Invention. The Examiner has characterized Applicant's Background as expressly teaching the step of selecting at least two chip assemblies for inclusion in a matched set based upon simultaneous testing. To the contrary, Applicant's background discloses assembling identical or dissimilar components as a matched set following the testing of each component individually, not simultaneously. Specifically, the Applicant states the following in the Background of the Invention:

> One approach for improving system performance is through the use of matched sets. For example, several identical

> or dissimilar components that have been identified by the **individual testing phase** of component processing to have certain performance tracking characteristics may be assembled together as a matched set. The components of such a matched set are frequently attached to a single substrate in close proximity to one another. This strategy improves performance compared to conventional or non-optimized systems by reducing the overall space needed to accommodate the chips and by, among other things, shortening the distance between chips. Specifically, interconnect inductance and signal transmission delays are all reduced.
>
> One type of matched set includes a collection of identical components which have been identified to meet specific system performance requirements....Typically, each of the identical components has been extensively **tested individually** prior to inclusion in this type of system....[M]ulti-dimensional arrays of data are then compared to each other to identify individual components that perform within acceptable limits relative to each other. Components that are found to exhibit similar behavior under the various input stimuli will constitute a matched set of identical devices. Conversely, components that are found to exhibit dissimilar behavior under the various input stimuli...will constitute a mismatch of components that will not be placed in a chip collection.
>
> It has been found, however, the certain mismatches are not identified when the components are tested individually. In fact, certain mismatches are not identified until the entire chip collection is assembled and the components are **tested together for the first time**. Emphasis added. Page 2, line 20 - Page 4, line 10.

During the course of discussing the individual testing of components, Applicant states the following: "each of the individual components has been extensively **tested individually prior** to inclusion in the system;" "certain mismatches are not identified when the components are **tested individually**;" and "certain mismatches are not identified until the entire chip

collection is assembled and the components are **tested together for the first time.**" Applicant's background neither discloses nor suggests selecting components based upon simultaneous testing. To the contrary, Applicant's Background of the Invention discusses the long felt need for improving the matched set component selection process and identifies the limitations of testing components individually. Applicant respectfully submits that the Examiner has inappropriately characterized Applicant's background as disclosing the step of selecting at least two chip assemblies for inclusion in a matched set based upon the simultaneous testing of the integrated circuit chips of the semiconductor wafer.

Accordingly, even if Lam and Applicant's Background of the Invention were combined as proposed by the Examiner, the method for selecting components for a matched set as recited in claim 1 would not be found in the combination. In particular, the step of "selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing" is not found in the combination. Therefore, Lam and Applicant's Background of the Invention do not disclose the method for selecting components for a matched set as recited in claim 1. Accordingly, Applicant

respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 1.

Claims 2-17 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2-17 is respectfully requested.

The present invention, as defined by independent claim 18, is directed to a method for assembling a matched set. Similar to claim 1, claim 18 includes limitations directed to providing a semiconductor wafer having a plurality of integrated circuit chips, coupling the wafer to an interposer to form a wafer-interposer assembly, and simultaneously testing pairs of the integrated circuit chips of the wafer for inclusion in a matched set based upon the testing. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 18.

Claims 19-34 depend from independent claim 18 and introduce further limitations in combination therewith. Therefore, the allowance of claims 19-34 is respectfully requested.

The present invention, as defined by independent claim 35, is directed to a matched set assembled by the method as recited in claim 18. Accordingly, for the reasons presented

hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 35.

The present invention, as defined by independent claim 36, is directed to a matched set of integrated circuit chips. Similar to claim 1, claim 36 includes limitations directed to simultaneously testing first and second chip assemblies that are a part of a wafer-interposer assembly for inclusion in a matched set based upon the testing. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 36.

Claims 37-41 depend from independent claim 36 and introduce further limitations in combination therewith. Therefore, the allowance of claims 37-41 is respectfully requested.

Fee Statement

Form PTO-2038 is submitted herewith authorizing the Commissioner to charge $55.00 to the indicated account for an Extension for Response within First Month per 37 C.F.R. §1.17(a)(1). Accordingly, Applicant believes no additional fees are due for the filing of this Response. However, if any additional fees are due, or any overpayments have been made, please charge, or credit, our Deposit Account No. 03-1130.

Conclusion

In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejection to claims 1-41 and allow claims 1-41 presented for reconsideration herein. Accordingly, a favorable action in the form of a Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 23rd day of October, 2002.

Respectfully submitted:

Lawrence R. Youst
Reg. No. 38,795
Danamraj & Youst, P.C.
12900 Preston Road
Suite 1200, LB-15
Dallas, Texas 75230
Tel 972.392.2696
Fax 972.720.1139

Marked Up Claims per 37 C.F.R. §1.121(c)(1)(ii)

No claims have been amended by way of the present Response. Accordingly, no marked up claims are believed to be necessary.